WHAT IS CLAIMED IS:

1. A method comprising:

detecting a reset condition;

verifying a memory controller is initialized; and

placing a memory system into a retention state.

2. The method of Claim 1, further comprising verifying the memory controller is initialized by delaying a reset signal.

3. The method of Claim 1, further comprising monitoring the voltage level of a system to determine a power failure.

4. The method of Claim 3, further comprising generating a reset condition when either a power failure or a reset request occurs.

5. The method of Claim 4, further comprising verifying the reset request does not occur prior to initialization.

6. The method of Claim 1, further comprising detecting the reset condition and verifying the memory controller is initialized external to the memory controller.

7. A memory system comprising:

a power delay circuit external to a memory controller, wherein the power delay circuit instructs the

memory system to run a retention routine during a power failure or reset condition.

8. The memory system of Claim 7, further comprising a power fail controller which prevents the retention routine from executing when the memory system is not configured.

9. The memory system of Claim 7, wherein the power delay circuit outputs a reset signal is either a power failure or a system reset signal is detected.

10. The memory system of Claim 9, wherein the power delay circuit outputs a delay signal when the output reset signal is caused by a system reset signal.

11. The memory system of Claim 7, wherein the power delay circuit monitors a voltage detector to detect a power failure.

12. The memory system of Claim 8, wherein the power fail controller may be internal to the memory controller.

13. A method placing a memory system in a data retention mode comprising:

detecting either a power failure or reset signal;

generating a delay signal based on the reset signal; and

initiating a data retention routine if the delay signal indicates the memory system is initialized.

14. The method of Claim 13 further comprising monitoring the voltage level of a system to determine a power failure.

15. The method of Claim 13, further comprising generating two output signals to the memory controller based on the delay signal.

16. The method of claim 13, further comprising preventing initiating the data retention routine if the reset signal is not de-asserted for a predetermined period of time.